General Description

The CT5504D is a high performance AC/DC power supply controller for battery charger and adapter applications. The CT5504D uses Pulse Frequency Modulation (PFM) method to build discontinuous conduction mode (DCM) fly-back power supplies.

The CT5504D provides accurate constant voltage, constant current (CV/CC) regulation without requiring an opto-coupler and the secondary control circuitry. The CT5504D can achieve excellent regulation and high average efficiency.

The CT5504D has a proprietary cable voltage drop compensation function. Internal random frequency modulation to reduce system EMI.

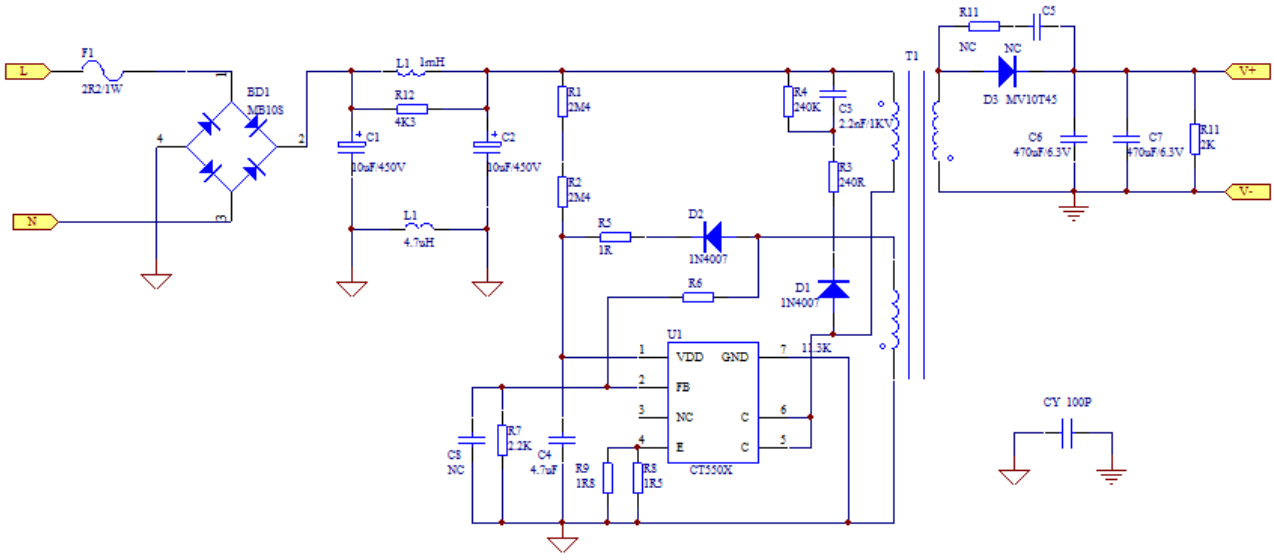
The CT5504D integrates functions and protections of Under Voltage Lockout (UVLO), VDD over Voltage Protection (VDD OVP), Cycle-by-cycle Current Limiting (OCP), Short Load Protection (SLP), On-Chip Thermal Shutdown, VDD Clamping, etc

The CT5504D is available in DIP-7 package.

Features

- Built-in 850V BJT
- Quasi-Resonant Primary Side Regulation (QR-PSR) Control with High Efficiency
- Standby power<70mw
- Low stat-up current <1uA
- High efficiency
- Multi-Mode PSR Control
- Fast Dynamic Response
- Built-in Dynamic Base Drive
- Audio Noise Free Operation
- ±5% CC and CV Regulation
- Programmable Cable Drop Compensation (CDC) in CV Mode
- Built-in AC Line & Load CC Compensation
- Build in Protections:
  - Short Load Protection (SLP)
  - Cycle-by-Cycle Current Limiting (OCP)
  - Leading Edge Blanking (LEB)
  - On-Chip Thermal Shutdown (OTP)
  - VDD OVP & UVP & Clamp

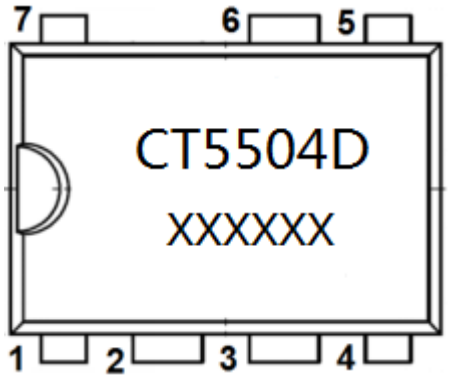
Typical Application



Ordering Information

Part Number	Package	Package Method	Marking
CT5504D（DIP-7）	DIP-7	Tube 50pcs/Tube	CT5504D XXXXXX

Pin Assignment



Pin Description

Pin	Pin Name	Description
VDD	1	IC Supply Voltage input
FB	2	Feedback input
NC	3	Not Connect
CS	4	Current sense input
C	5/6	Collector of internal BJT
GND	7	IC Ground

Recommended Operation Conditions

Part Number	230VAC ± 15%(2)	85-265VAC
CT5504D	Adapter(2)	Adapter(2)
	15W	12W

Note 1. The Max. output power is limited by junction temperature

Note 2. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern as a heat sink at 50℃ ambient.

Absolute Maximum Ratings

Parameter	Symbol	Parameter Range	Unit
C pin Voltage(C)	V_C	-0.3~850	V
Supply Voltage（VCC）	V_{VCC}	25	V
FB pin Voltage （FB）	V_{FB}	-0.7~7	V
CS pin voltage （CS）	V_{CS},V_E	-0.3~7	V
OUT pin output current	I_{OUT}	Internal limited	A
Maximum Power Dissipation (Ta=25°C)	P_{tot}	0.90@ DIP-7	W
Thermal Resistance Junction-ambient	Rthj-a	80@ DIP-7	℃/W
Operating Junction Temperature	T_J	-40～150	℃
Storage Temperature Range	T_{STG}	-55～150	℃
V_{ESD_HBM}	Human Body Model	2,000	V
V_{ESD_MM}	Machine Model	200	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability。

Recommended Operation Conditions

Parameter	Value	Unit
Supply Voltage, V_{CC}	7 to 21	V
Operating Ambient Temperature	-40 to 85	°C
Maximum Switching Frequency @ Full Loading	70	kHz
Minimum Switching Frequency @ Full Loading	35	kHz

Note2. The device is not guaranteed to function outside its operating conditions.

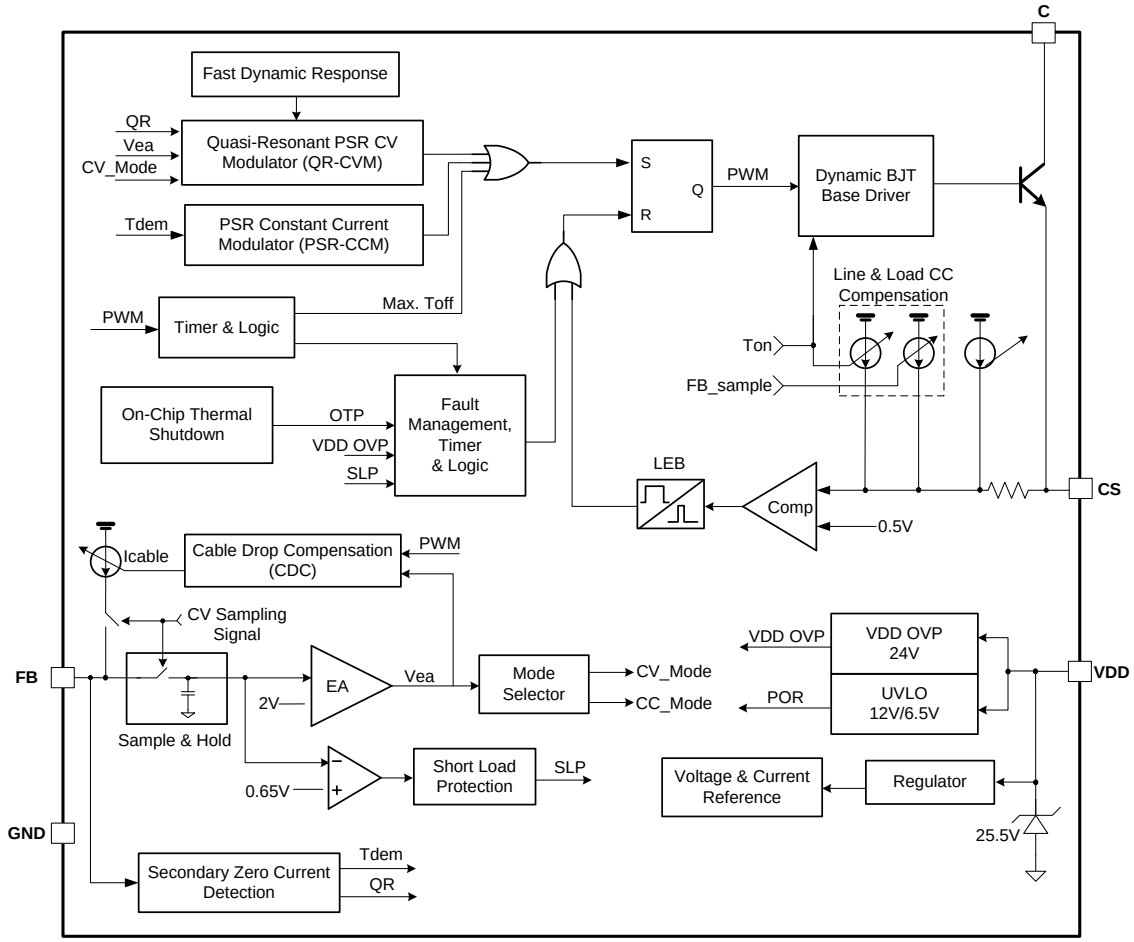
Electronic Characteristics

T_C =25°C,V_{CC} = 20V,unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage Section(V_{CC} Pin)						
I_{VCC_st}	Start-up current into V_{CC} pin			3	20	uA
I_{VCC_Op}	Operation Current			0.8	1.5	mA
$I_{VCC\_standby}$	Standby Current			0.5	1	mA
V_{CC_ON}	V_{CC} Under Voltage Lockout Exit		10.5	12	13.5	V
V_{CC_OFF}	V_{CC} Under Voltage Lockout Enter		5.5	6.5	7	V
V_{CC_OVP}	V_{CC} OVP Threshold		22	24	26	V
V_{CC_Clamp}	V_{CC} Zener Clamp Voltage	I(V_{CC}) = 7 mA	23.5	25.5	27.5	V
Control Function Section (FB Pin)						
V_{FBREF}	Internal Error Amplifier (EA) Reference Input		1.97	2.0	2.03	V
V_{FB_SLP}	Short Load Protection (SLP) Threshold			0.65		V
T_{FB_Short}	Short Load Protection (SLP) Debounce Time			36		ms
V_{FB_DEM}	Demagnetization Comparator Threshold			25		mV
T_{off_min}	Minimum OFF time			2		us
T_{on_max}	Maximum ON time			20		us
T_{off_max}	Maximum OFF time			5		ms
I_{Cable_max}	Maximum Cable Drop Compensation(CDC) Current			60		uA
T_{SW} /T_{DEM}	Ratio between Switching Period and Demagnetization Time in CC Mode			7/4		
Current Sense Input Section (CS Pin)						
T_{LEB}	CS Input Leading Edge Blanking Time			500		ns
$V_{cs(max)}$	Current limiting threshold		490	500	510	mV

T_{D_OC}	Over Current Detection and Control Delay			100		ns
Power BJT Section (C Pin)						
BV_{CBO}	Collector-Base Breakdown Voltage		850	-		V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	Ic=4.0A			1.20	V
Ic	Maximum Collector Current			4.0		A
On-Chip Thermal Shutdown						
T_Z	Intelligent Thermal Control Threshold	Output Power Shut Down	---	155	--	℃
T_{OTP}	OTP Threshold	Restart		140	--	℃

Functional Block Diagram



Applications Information

Functional Description

The CT5504D is a high performance, multi mode, highly integrated Quasi Resonant Primary Side Regulation (QR-PSR) power switch. The built-in high precision CV/CC control with high level protection features makes it suitable for offline small power converter applications.

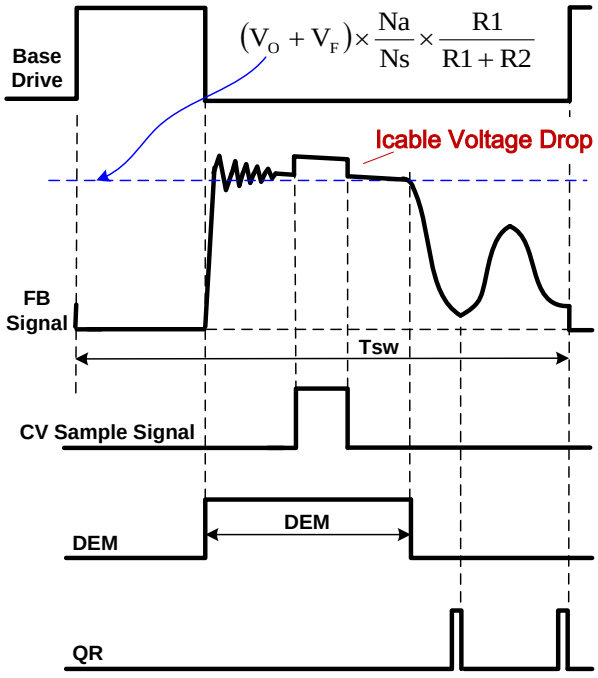
System Start-Up Operation

Before the IC starts to work, it consumes only startup current (typically 3uA) which allows a large value startup resistor to be used to minimize the power loss and the current flowing through the startup resistor charges the VDD hold-up capacitor from the high voltage DC bus. When VDD reaches UVLO turn-on voltage of 12V (typical), CT5504D begins switching and the IC operation current is increased to be 0.8mA (typical). The hold-up capacitor continues to supply VDD before the auxiliary winding of the transformer takes the control of VDD voltage.

Once CT5504D enters very low frequency FM (Frequency Modulation) mode, the operating current is reduced to be 500uA typically, which helps to reduce the standby power loss.

Quasi Resonant PSR CV Modulation (QR-CVM)

In Primary Side Regulation (PSR) control, the output voltage is sensed on the auxiliary winding during the transfer of transformer energy to the secondary. Following Fig. illustrates the timing waveform of CV sampling signal, demagnetization signal (DEM) and quasi-resonant (QR) trigger signal in CT5504D. When the CV sampling process is over, the internal sample/hold (S&H) circuit captures the error signal and amplifies it through the internal Error Amplifier (EA). The output of EA is sent to the Quasi Resonant PSR CV Modulator (QR-CVM) for CV regulation. A valley is selected to trigger new PWM cycle by the output of the QR-CVM bock, which is determined by the load. The internal reference voltage for EA is trimmed to 2V with high accuracy.



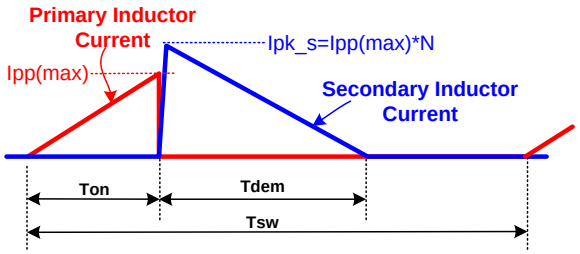
During the CV sampling process, an internal variable current source is flowing to FB pin for Cable Drop Compensation (CDC). Thus, there is a step at FB pin in the transformer demagnetization process, where Vo and VF is the output voltage and diode forward voltage; R1 and R2 is the resistor divider connected from the auxiliary winding to FB Pin, Ns and Na are secondary winding and auxiliary winding respectively.

When heavy load condition, the Mode Selector (as shown in “Block Diagram”) based on EA output will switch to CC Mode automatically.

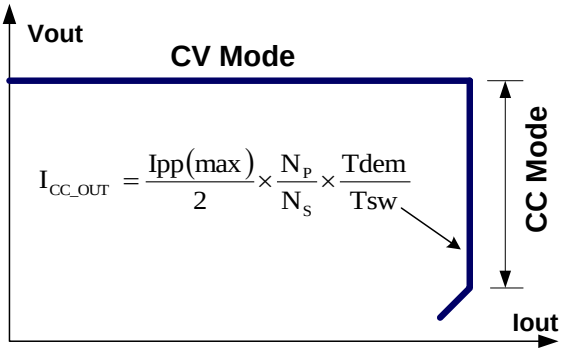
PSR Constant Current Modulation (PSR-CCM)

Timing information at the FB pin and current information at the CS pin allow accurate regulation

of the secondary average current. The control law dictates that as power is increased in CV regulation and approaching CC regulation the primary peak current is at Ipp(max), as shown in Fig. on the right.



Referring Fig. on the rght, the primary peak current, transformer turns ratio, secondary demagnetization time (Tdem), and switching period (Tsw) determines the secondary average output current Iout. Ignoring leakage inductance effects, the equation for average output current is shown. When the average output current Iout reaches the regulation reference in the Primary Side Constant Current Modulator (PSR-CCM) block, the CT5504D operates in pulse frequency modulation (PFM) mode to control the output current at any output voltage at or below the voltage regulation target as long as the auxiliary winding can keep VDD above the UVLO turn-off threshold.



In CT5504D, the ratio between Tdem and Tsw in CC mode is 4/7. Therefore, the average output current can be expressed as:

$$I_{CC\_OUT}(mA) \cong \frac{2}{7} \times N \times \frac{500mV}{Rcs(\Omega)}$$

Where,

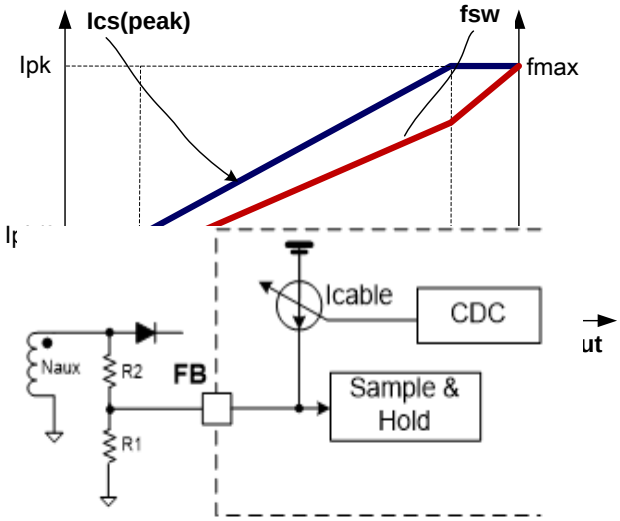
N----The turn ratio of primary side winding to secondary side winding.

Rcs--- the sensing resistor connected between the power BJT emitter to GND.

Multi Mode Control in CV Mode

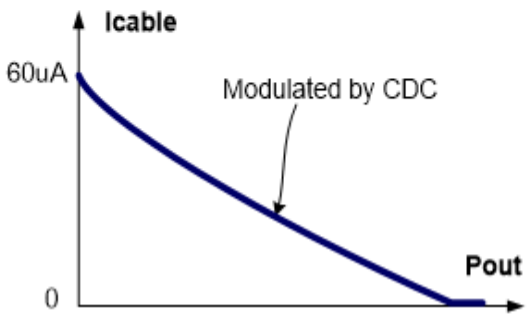
To meet the tight requirement of averaged system efficiency and no load power consumption, a hybrid of frequency modulation (FM) and amplitude modulation (AM) is adopted in CT5504D which is shown in the below Fig.

Around the full load, the system operates in FM mode. When normal to light load conditions, the IC operates in FM+AM mode to achieve excellent regulation and high efficiency. When the system is near zero loading, the IC operates in FM again for standby power reduction. In this way, the no-load consumption can be less than 70mW.



Programmable Cable Drop Compensation (CDC) in CV Mode

In smart phone charger application, the battery is always connected to the adapter with a cable wire which can cause several percentages of voltage drop on the actual battery voltage. In CT5504D, an



offset voltage is generated at FB pin by an internal current source (modulated by CDC block, as shown in Fig. on the right) flowing into the resistor divider. The current is proportional to the switching period, thus, it is inversely proportional to the output power Pout. Therefore, the drop due the cable loss can be compensated. As the load decreases from full loading to zero loading, the offset voltage at FB pin will increase. By adjusting the resistance of R1 and R2 (as shown in Fig. on the right), the cable loss compensation can be programmed. The percentage of maximum compensation is given by

$$\frac{\Delta V(cable)}{Vout} \approx \frac{Icable\_max \times (R1//R2)}{V_{FB\_REF}} \times 100\%$$

For example, R1=3KΩ, R2=18KΩ, The percentage of maximum compensation is given by:

$$\frac{\Delta V(cable)}{Vout} = \frac{60uA \times (3K//18K)}{2V} \times 100\% = 7.7\%$$

Fast Dynamic Response

In CT5504D, the dynamic response performance is optimized to meet USB charge requirements.

On Chip Thermal Shutdown (OTP)

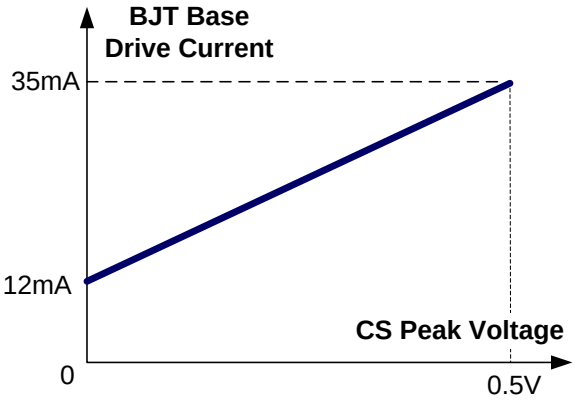
When the CT5504D temperature is over 155℃, the IC shuts down. Only when the IC temperature drops to 140℃, IC will restart.

Audio Noise Free Operation

As mentioned above, the multi-mode CV control with a hybrid of FM and AM provides frequency modulation. An internal current source flowing to CS pin realizes CS peak voltage modulation. In CT5504D, the optimized combination of frequency modulation and CS peak voltage modulation algorithm can provide audio noise free operation from full loading to zero loading.

Dynamic BJT Base Drive

CT5504D integrates a dynamic base drive control to optimize efficiency. The BJT base drive current ranges from 12mA to 35mA (typical), and is dynamically controlled according to the power supply load change. The higher the output power, the higher the based current. Specifically, the base current is related to CS peak voltage, as shown in Fig in the right.



Short Load Protection (SLP)

In CT5504D, the output is sampled on FB pin and then compared with a threshold of UVP (0.65V typically) after an internal blanking time (36ms typical).

In CT5504D, when sensed FB voltage is below 0.65V, the IC will enter into Short Load Protection (SLP) mode, in which the IC will enter into auto recovery protection mode.

VDD Over Voltage Protection (OVP) and Zener Clamp

When VDD voltage is higher than 24V (typical), the IC will stop switching. This will cause VDD

fall down to be lower than VDD_OFF (typical 6.5V) and then the system will restart up again. An internal 25.5V (typical) zener clamp is integrated to prevent the IC from damage.

Frequency Shuffling function

The CT5504D has built-in frequency shuffling function to reduce system EMI.

DIP-7 MECHANICAL DATA

UNIT：mm

SYMBOL	min	nomarl	max	SYMBOL	min	nomarl	max
A	9.00		9.20	C2		0.50TYP	
A1	1.474		1.574	C3	3.20		3.40
A2	0.41		0.51	C4	1.47		1.57
A3	2.44		2.64	D	8.20		8.80
A4		0.51TYP		D1	0.244		0.264
A5		0.99TYP		D2	7.62		7.87
B	6.10		6.30	Θ1		17°TYP4	
C	3.20		3.40	Θ2		10°TYP4	
C1	7.10		7.30	Θ3		8°TYP